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January 9, 2002

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

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FEB 04 2002
GROUP 3600

Subject:

Serial No. 09/989,837 11/20/01

Chao Chieh Tsai, Shih-Chih Wong

RF SEAL RING STRUCTURE

Grp. Art Unit: 3626

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner of Patents and
Trademarks, Washington, D.C. 20231, on January 22, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

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Technology Center 2100

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TECHNOLOGY CENTER 2800

U.S. Patent 5,717,245 to Pedder, "Ball Grid Array Arrangement," teaches a system using a dielectric multi-layer substrate where RF interference is reduced by grounding certain areas and encapsulating the substrate within a conductive seal ring.

U.S. Patent 6,028,497 to Allen et al., "RF Pin Grid Array," teaches a system where RF signals are passed through a network of holes in the base plate of the module.

The following two U.S. Patents teach methods employing a leadless chip carrier package where a grounded conductor protrudes between input and output signal pads thereby preventing interference:

- 1) U.S. Patent 5,864,092 to Gore et al., "Leadless Ceramic Chip Carrier Crosstalk Suppression Apparatus."
- 2) U.S. Patent 6,105,226 to Gore et al., "Leadless Ceramic Chip Carrier Crosstalk Suppression Method."

U.S. Patent 5,998,245 to Yu, "Method for Making Seal-Ring Structure with ESD Protection Device," teaches a method where ESD protection is incorporated into a seal ring structure on an IC die.

U.S. Patent 6,028,347 to Sauber et al., "Semiconductor Structures and Packaging Methods," teaches a method where a portion of the seal ring is formed in trenches in the semiconductor surface.

U.S. Patent 5,185,654 to Mosher et al., "Electrostatic RF Absorbant Circuit Carrier Assembly and Method for Making the Same," teaches a method using a circuit carrier to encapsulate a circuit while absorbing RF and hi-voltage electrostatic discharge (ESD) signals.

U.S. Patent 4,868,716 to Taylor et al., "RF Interconnect and Shielding System," teaches a method using a pin grid assembly with a back plane to encapsulate circuit modules and prevent RF propagation between modules.

U.S. Patent 6,180,876 to Holmes, "Apparatus and Method for RF Shielding of a Printed Circuit Board," teaches a method using grounded conductive partitions on a circuit board to isolate different circuitry.

Sincerely,

A handwritten signature in black ink, appearing to read 'SBA', is written over the printed name.

Stephen B. Ackerman,
Reg. No. 37761